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# LOW POWER VLSI TECHNIQUES FOR PORTABLE DEVICES

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**Abstract:**
*In the present day scenario, designing a circuit with low power has become very important and challenging task. The designing of any processor for portable devices demands low power. This can be achieved by incorporating low power design strategies and rules at various stages of design. To increase the performance of portable devices, the power backup should be taken in consideration, which is extremely desirable from the users prospective. As we approaches towards the sub-micron technology the requirement of low power devices increases significantly. But at the same time leakage current and dynamic power dissipation play a vital role to diminish the performance of portable devices. This paper presents techniques to reduce the power dissipation and various methodologies to increase the speed of device. That is very beneficial for designing of future VLSI circuits.*

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## 1. Introduction

Today more than 95 % of VLSI chips are made out of silicon. There are millions of transistors housed in this small chip. Silicon is a Group IV element semiconductor. It has a number of very desirable properties. The VLSI chip currently in the market is made of silicon and that too single crystal silicon. When talking about very high-speed circuits, we usually have them in bipolar junction transistors. BJT's have very high speed and when using about very high packing density, we usually used MOSFET like the DRAM chip. This is based on MOSFET technology, million transistors in a given area of integrated circuit and given area of silicon. The growth rate of chip shown in figure 1.

Essentially VLSI technology divided in two branches. One is BJT technology and the other is MOSFET technology. The technology of processor clock rate has increased starting with 167 megahertz to 1,000 megahertz and most of the processors are now operating in the range of gigahertz. Now in the advancement of technology that means the size is gradually shrinking starting with 0.45 micron to 0.25 micron. The area of current technology processor is 60 nanometers to 45 nanometers. If keep on decreasing the size of processor, the supply voltage and power dissipation will reduce, but the peak power dissipation has increased from 30 to 100 watts.

Power consumption has been a major concern on microprocessor. To overcome related to power dissipation problem, many scientists and researchers have proposed from the device level to the architectural level [4].
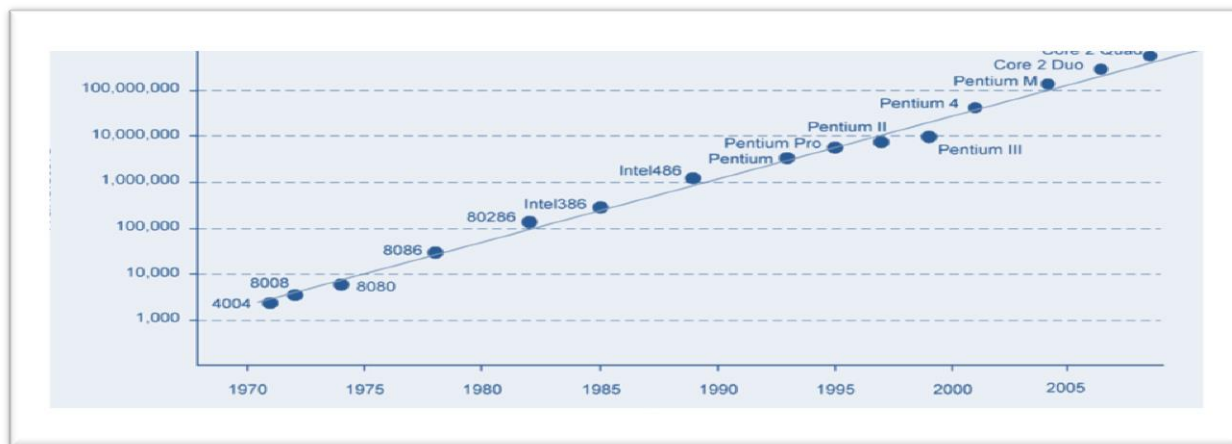


Figure 1: Growth rate of transistor on chip

Most of the processors used now a day's high-performance processors consume 100 watts. So, must be needed effective cooling and packaging technique because of the power dissipation, therefore need to develop very sophisticated packaging and cooling technique. On this paper explain various power dissipation causes of power consumption, and proposed possible solutions to minimize power dissipation in a CMOS device.

## 2. Source of Power Dissipation in Cmos and Control Techniques

The sources of power dissipation in CMOS circuits can be broadly divided into two types, dynamic power and static power. The main difference between dynamicpower and static power; dynamic power is essentially when the circuit is in operation or circuit is in in action and doing some processing. Static power is when the circuit is in the standby mode some circuits are not in use it can be switched to standby mode [5].

The various power dissipation on microprocessor distribution shown on fig. 2. The repeated charging and discharging of the output capacitance is necessary to transmit information in CMOS circuits. The charging and discharging causes for the switched power dissipation. The power consumption of a CMOS digital circuit can be represented as

$$P = fCV_{dd}^2 + fI_{short}V_{dd} + I_{leak}V_{dd}$$

Where f is the clock frequency, C is the average switched Capacitance per clock cycle, $V_{dd}$ is the supply voltage, $I_{short}$ is the short circuit current and $I_{leak}$ is the leakage current.
The total power dissipation of a logic cell can be described as follows:

$P_{total} = P_{active} + P_{leak} = P_{dyn} + P_{SC} + P_{leak}$

Where: $P_{leak}$ is the power consumed during the steady-state period, and $P_{active}$ is the power dissipated during logic transitions. The dynamic power $P_{dyn}$ and the short-circuit power $P_{SC}$.
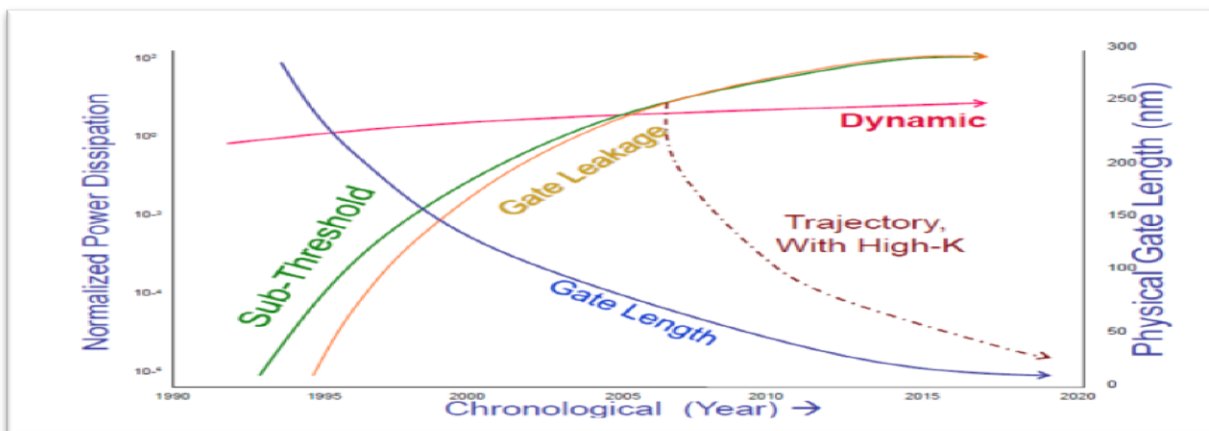


Figure 2: Power Dissipation Distributions

## 2.1. Switching Power Dissipation

CMOS circuit there is a lot of capacitances. It is gate capacitance and interconnects capacitance. Various types of capacitances are present in a circuit and those capacitances gets charged and discharged during normal circuit operation. It leads to power dissipation and that is known as the switching power dissipation. There is a pull-up Network made of pMOS transistors and there is a pull-down network made of nMOS transistors [6]. As shown on fig.3&4
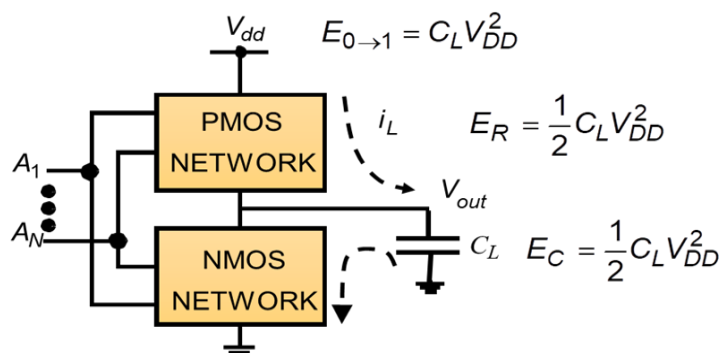


Figure 3: CMOS pull-up and pull-down network [6]

A complex CMOS circuit contains billions of capacitive circuit nodes, nodes that are charged and discharged during switching thereby dissipating power. All these node capacitors are charged through p-channel devices in the pull-up network, and discharged through n-channel devices in the pull-down network [2]. Power dissipation per charge or discharge can be expressed by equation.

$$P_{dyn} = \alpha C_L V^2_{DD} f$$

Where, P is the power consumed, $\alpha$ activity factor, C the switched load capacitance, V the supply voltage and f the clock frequency. A clock in a system has activity factor of $\alpha$ = 1, since it rises and falls every cycle. Mostly the activity factor of the data is 0.5. Dynamic power dissipation can be computed effectively if the right load capacitance estimated at the nodes and by factoring in the activity factors [2].
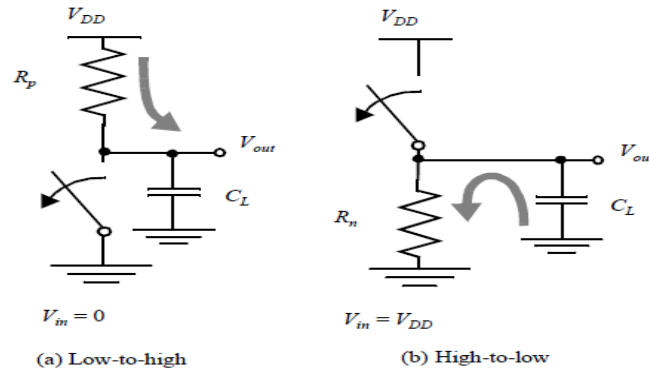


Figure 4: CMOS inverter used in the dynamic power-dissipation analysis

## 2.2. Shortcircuit Power Dissipation

Second type of power dissipation dynamic power dissipation is known as short-circuit power dissipation. CMOS circuit when the output is 1 then the pMOS network path is on and circuit is open, but the nMOS network path is closed and circuit is on. The other hand when the output is 0 the nMOS network path is open, the pMOS network path is closed [4]. In other words there is no direct path from supply to ground. Shown in figure 5.

This is a simple inverter circuit; when the input is 1 nMOS is on, when the input is 0 pMOS is on, but normally for low and high inputs there is no direct path from the supply voltage to ground. There should not be any short circuit path, short-circuit current passing through the transistor but when the input changes slowly from 0 to 1 or low to high or from high to low, there is a region in between where both the transistors are on.
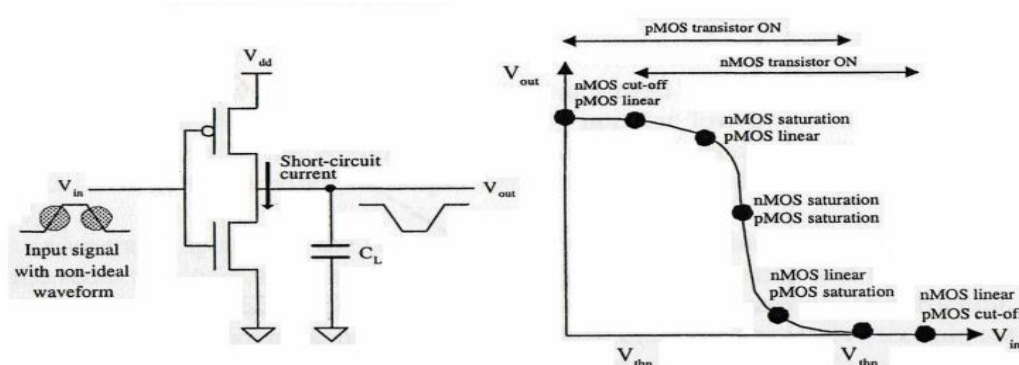
Figure 5: CMOS inverter short-circuit current (pMOS and nMOS simultaneously on during transition)

When the input voltage is greater than the threshold voltage of the nMOS transistor and less than the threshold voltage than $V_{DD}$ minus threshold voltage of the pMOS transistors, for that time of the input both the transistors will be on, and as a consequence there is a short circuit path from supply to ground [5]. This is known as short circuit power dissipation. As shown oncharacteristic due to Direct-Path Currents in figure 6.

The short-circuit power dissipation is given by

$$P_{SC} = \frac{\beta}{12}(V_{dd} - 2V_T)^3 \frac{\tau}{T}$$

The formula describes the short-circuit power dissipation in a CMOS inverter without output load, where β is the gain factor, τ is the input rise/fall time of inverter and T is the input signal period.
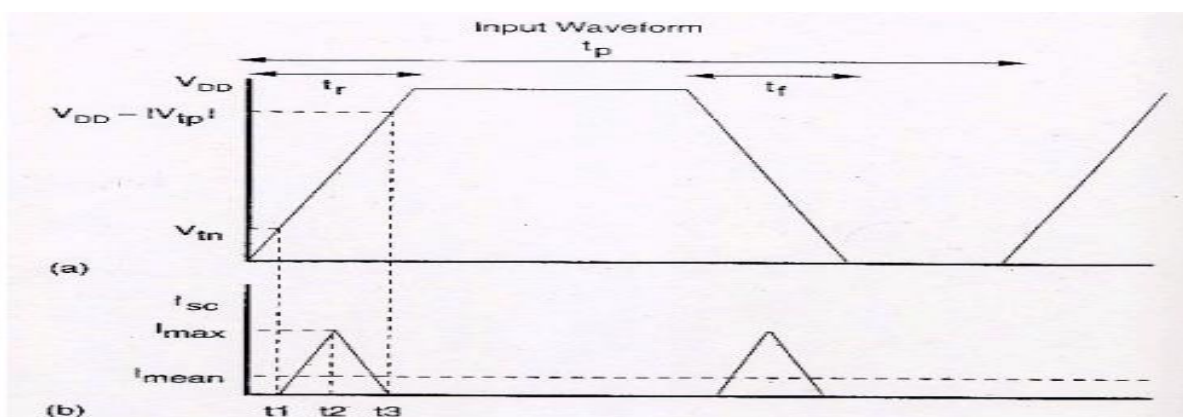


Figure 6: VI characteristic due to Direct-Path Currents

There is strong dependence on frequency and there is dependence on the rise time and fall time. Slow rise times on nodes can result in significant (20%) short-circuit power dissipation for loaded inverters. It is good practice to keep all edges fast, if power dissipation is a concern.
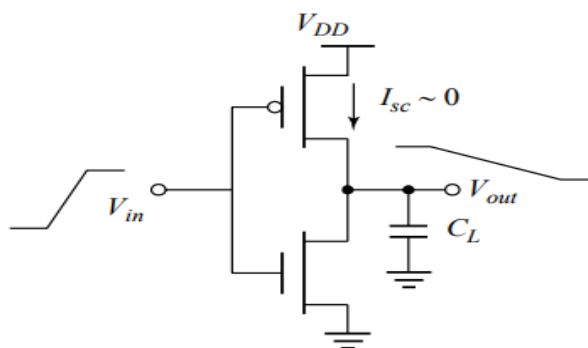
Figure 7: Impact of load capacitance on short-circuits current (Large Capacitive load)

If assume that on first case on figure 7, the load capacitance is very large, on that condition the output fall time is significantly larger than the input rise time. Therefore short-circuit current is close to zero. Now on reverse case on fig.8, where the output capacitance is very small, and the output fall time is substantially smaller than the input rise time. The voltage of drain-source in pMOS device equals $V_{DD}$ for most of the transition period, so the maximal short-circuit current.This analysis leads to the conclusion that the short-circuit dissipation is minimized by making the output rise/fall time larger than the input rise/fall time [3].
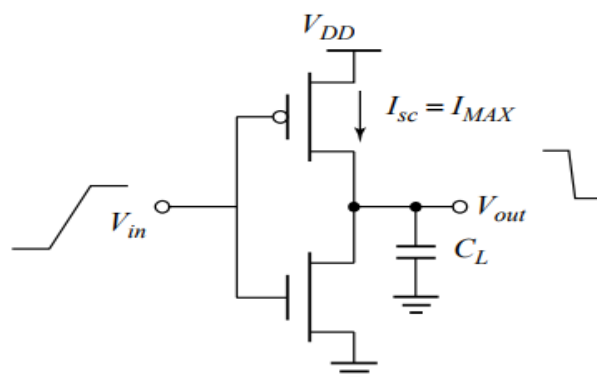


Figure 8: Impact of load capacitance on short-circuits current (Small capacitive load)

On the other hand, making the output rise/fall time too large slows down the circuit and can cause short-circuit currents shown on waveform in fig.9.
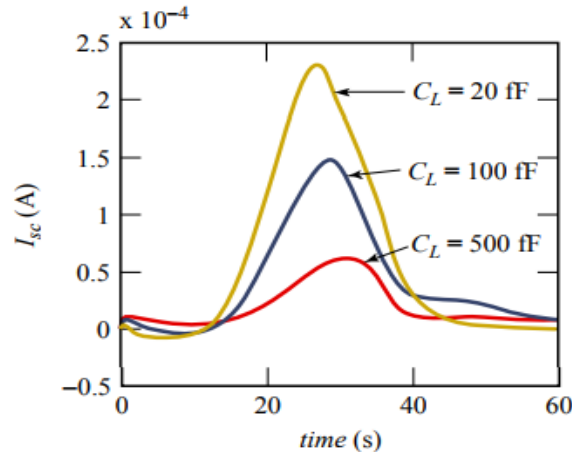
Figure 9: CMOS inverter short-circuit

## 2.3. Static Power Dissipation

Leakage power dissipation, we know that standby power is essentially known as leakage power. When the circuit is in standby mode, the inputs are not changing. The circuit is in standby mode, but the circuit is connected to the supply voltage and as a result, it will lead to some power dissipation. It is primarily due to leakage current. This is a typical MOS transistor; here is the mention leakage current I1 to I5 contribution diagram on fig.10.
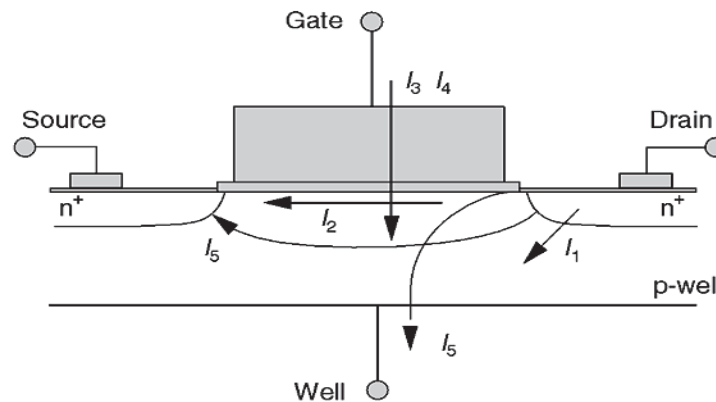


Figure 10: Leakage current contributions

The typical CMOS inverter as per diagram 11, combination of nMOS transistor & pMOS transistor. The nWell and p-type substrate made the combination of P & N type substrate. Therefor it considers as a diode. It forms a diode and these diodes arereverse biased. When a diode is reverse-biased, it will have some reverse bias current. It is shown on fig.12.
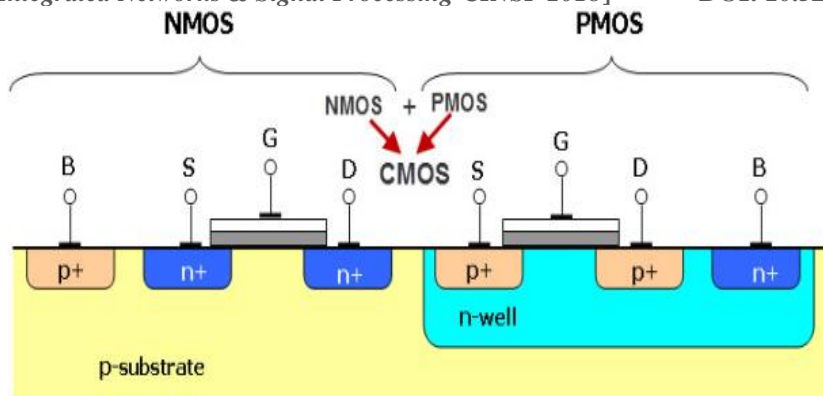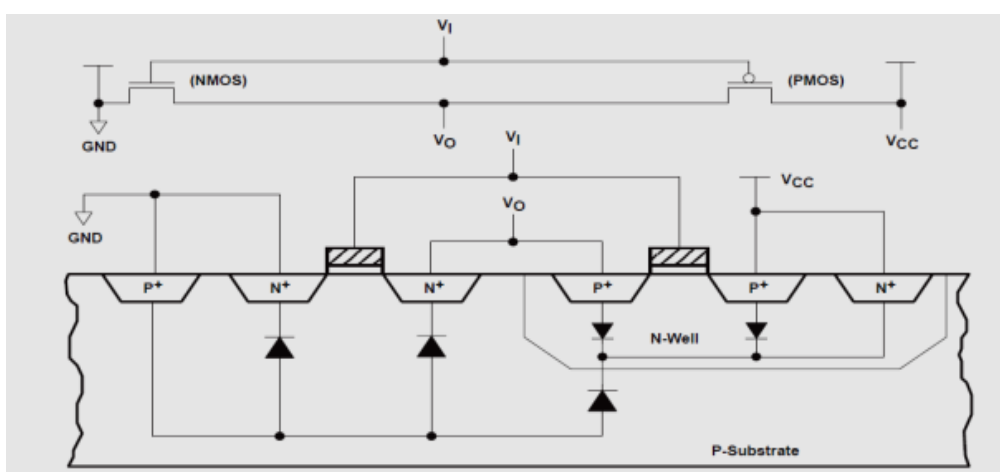
Figure 11: CMOS inverter


Figure 12: Model Describing Parasitic Diodes Present in CMOS Inverter [2].

The current for one diode is given by

$$I_{lkg} = i_s \left( e^{qV/Kt} - 1 \right)$$

Where:
$i_s$ = reverse saturation current
V = diode voltage
k = Boltzmann's constant ($1.38 \times 10^{-23}$ J/K)
q = electronic charge ($1.602 \times 10^{-19}$ C)
T = temperature
Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption $P_S$, can be obtained as shown in eq.

$$P_S = \sum (\text{leakage current}) \times (\text{supply voltage})$$

This static power consumption $P_S$, can be calculated by equation

$$P_s = V_{CC} \times I_{CC}$$

Where:
$V_{CC}$ = supply voltage
$I_{CC}$ = current into a device (sum of leakage currents as in equation 2)

The leakage current is dependent on temperature, active area of the device and reverse saturation current density. There are many transistors within a chip so take into consideration all the transistors. It has several million or a billion transistor within a chip now days. If sum up all the currents passing through it. So if have 1 million transistors then this current is roughly equal to 0.1 micro volts. It is 1 billion then it will become thousand times of that then, it cannot really ignore any longer. When the number of transistors is small, it can be ignored, but when the number of transistors within a chip is very large, then the current due to these reverse biased diodes will be quite large [2].
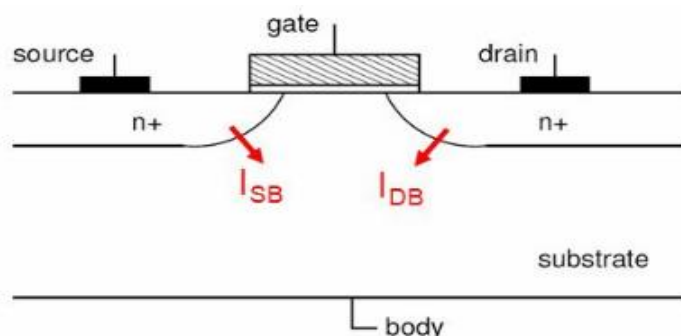


Figure 13: Band to Band Tunneling Current

The second type of current is known as band-to-band tunneling current that occurs because the size of the transistorsare sinking. Although the voltage across the gate and substrate or drain to source is very small 1.8 volt or 1 volt nowadays. The transistors size is very small about 60 nanometer because of this band-to-band tunneling occurs high electric field across the reverse bias PN Junction, causes significant current known as VT current or band-to-band tunneling. The electrons move from the valence band to the conduction band leading to current across the PN Junction. This is the expression for the band-to-band tunneling current. It is shown on fig.13 band to band tunneling current [5].

### 3. Conclusions

Electronic design aims at striking a balance between performance and power efficiency. We tried to relate general-purpose low-power design solutions to successful chips that use them to various extents. The current need of every system is to have low power dissipations in various fields and various systems. After study on the switching power and the leakage power, observe that both of these powers are dependent on the power supply voltage $V_{dd}$. The switching power has squared dependence of the power, therefore need the requirement is scale down the power supply voltage. It is the best techniques to reduce the voltage by implementing the architecture driven device voltage scaling based system.  These are pipelining and parallelization power reduction

techniques. Low-power methodology is very important to achieve goal. If we able to reduce power dissipation the cost associated with packaging and cooling will reduce and overall system performance will increase. It is important to develop low-power methodology to reduce the cost of packaging and cooling.

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