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FIN-FET BASED HIGH GAIN OP-AMP WITH SLEW RATE ENHANCEMENT IN 45-NM REGIME

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Abstract:
In this paper dynamic biasing technique is used for the enhancing the slew rate of the designed Op-Amp. The proposed FinFET based Op-Amp has been verified through Hspice simulator in the standard 45nm Silicon on Insulator FinFET library. The proposed op amp has two stages Miller compensated configuration. A biasing circuit (DSB circuit) is used for dynamic switching of the biasing voltage of the op amp. This leads to lower power consumption, wide ICMR range, and high gain stability. The proposed op amp has a power consumption of 661.83 µW. It has a dual supply voltage of -1.0V and 1.0V. The input common mode range (ICMR) is -800 mV to +900 mV. The Op-Amp has a slew rate of 1.5 KV/µs. Voltage gain of the op amp is 90.4dB. Due to the use of SOI FINFET devices the op amp has relatively less leakage current as compared to similar bulk MOSFET device op amps. The op amp has unity gain bandwidth of 1.27 GHz. Thus, it can be used to transmission and processing of audio and video signals.

Keywords: Slew Rate; Dynamic Biasing Circuit; Op-Amp; Unity Gain Bandwidth; Compensation Capacitor.

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1. Introduction

Op-amp is versatile and widely used in all modern instrumentation, communication, and sensor systems, etc. For sensor system where the output switches from one level to another quickly is required. In these applications the rate at which the op amp can change between the two levels is important that is input and output level. Therefore, high slew rate based op-amp architecture should be required. This motivates developing special architecture, which improve op-amp slew rates.

The maximum rate of output excursion defines the slew rate of an amplifier's. The maximum change in the output voltage with respect to per unit time is defined as slew rate. The limitation of slew rate is that it can increase the effect of nonlinearity in op-amp. The output of the op-amp cannot able to rise instantaneously to the input voltage at ideal value. The output will be a linear ramp of slope equal to SR. Then its output is slew rate limited and it said to be slewing. If signals

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will become distorted, i. e. op amp is operated above its slew rate limit. Slew rate also influences achievable performance in sensor system,filters, D/A output stages and video amplification.

$$SR = \frac{dv_o}{dt}$$

Due to the different internal circuitry of op amp arises the slew rate. There are two main reasons, which is responsible for the limitations of op amp chips [1].

A number of techniques have been proposed in the literature to enhance the gain of the FC OTA. One of these techniques presented in [3-4] enhances the DC gain by providing an additional current path at the cascode node. This converts the current source into active current mirror which raises the output current to be above its quiescent value during slewing. Another technique proposed in [5], enhances the DC gain and UGB by modifying the bias current sources of the FC OTA. These current sources do not contribute to DC gain. A recycling technique is proposed to overcome this disadvantage. This OTA is referred to as Recycling Folded Cascode (RFC). In [6], further enhancement in the DC gain and UGB of the RFC OTA is obtained using Improved Recycling structure and is termed as IRFC OTA. In this paper, an enhanced IRFC (EIRFC) OTA is proposed, by adopting the technique proposed in [3- 4] for the FC OTA. The performance of the two OTAs (IRFC and EIRFC) are evaluated through simulation and compared.

Basic Principles

The bias current source is directly proportional to the slew rate of op-amp in the first stage, which will increase the power dissipation of the circuit. The objective of the presented in this paper is to achieve a high slew rate, with a low power overhead while maintaining other performance of op-amp unchanged [9]. The internal architecture of the op amp is responsible for the slew rate.

Due to limited bandwidth of the op-amp, there are linear phenomenon occurred I. e. It does not lead nonlinear distortion. When an op-amp connected in unity gain configuration, the output would be expected from the follower if the only limitation on its dynamic performance is the finite op-amp bandwidth. The transfer function of unity gain op-amp [10-11].

$$\frac{V_O}{V_i} = \frac{1}{1 + {}^{S}/_{\omega_t}}$$

Which is low pass STC response with a time constant ${}^{1}/_{\omega_t}$. Therefore the step response should be $V_o(t) = V(1 - e^{-\omega_t t})$. Due to different circuit configuration of op amps, it may have different slew rates for positive and negative transitions. The different configuration of op-amp is responsible for the different slew rate. They have a complementary output to pull the signal up and down and i.e. the circuit cannot be exactly the same at two sides. [1].

2. Materials and Methods

The block diagram of proposed high slew rate operational amplifier is shown in fig. 1. In today's scenario, we require high slew rate as well as low power consumption in Op-Amps. Slew Rate

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depends upon two parameter current and load capacitance but we cannot play with load capacitance. Only design parameter Iss current can be changed but if we increase current steadily

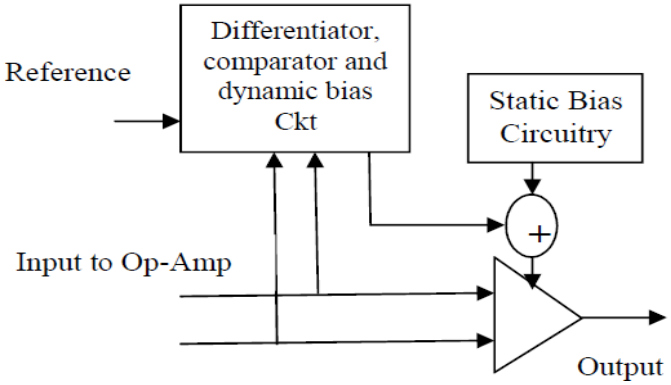

Figure 1: Block Diagram of proposed High Slew Rate Op-amp

then power dissipation will increases. So one other solution to reduce this higher power dissipation is to incorporate a dynamic current source that can provide a dynamic current flow during charging and discharging of capacitance otherwise normal current flow. So power dissipation is somewhat controllable. But our other circuit parameter should not be changed. We have divide design procedure in two parts:

2.1. Design of FINFET based Operational Amplifier

The circuit diagram of the proposed SOI FinFET based opamp is given in fig. 2. In this circuit, transistor M1, M2, M3 and M4 forms a differential amplifier. The output of this differential amplifier is then fed to a common source amplifier. Transistor M5 and M7 forms this common source amplifier. Transistor M6, M7 and M8 forms a current mirror which works as biasing circuit. Cc is the Miller compensation capacitor and C_L is load capacitor.

As shown in fig. 3 both input of the main Op-Amp circuit are connected in dynamic bias circuit. Consider Vin+ input, we first require differentiator so when out input speed is high then our circuit become active. Here, we take square wave input for checking purpose. So our differentiator gives spike in output. This spike output depends on the differentiator circuit. RC circuit is used as differentiator circuit in which output depends upon three parameters R, C and input speed (rise time and fall time). So these three are our design parameter.

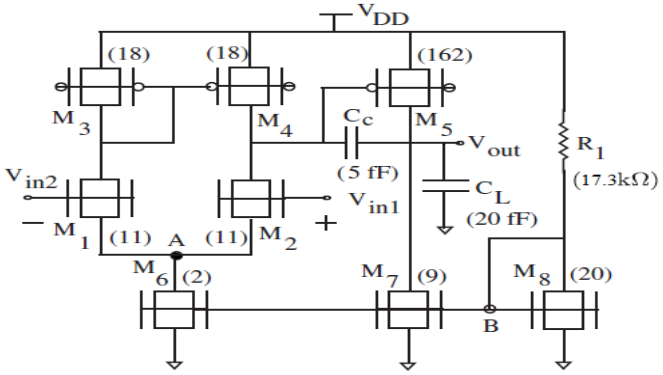

Figure 2: Fin-Fet based compensation Op-Amp.

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2.2. Proposed Dynamic Bias Circuit.

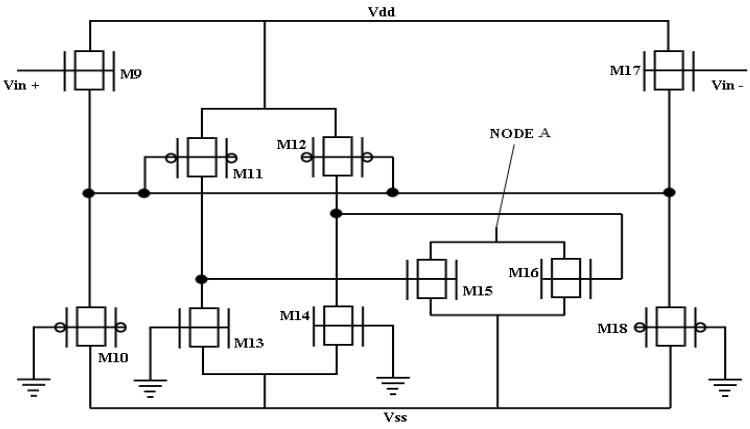

Figure 3: Dynamic Bias Circuit

We design the circuit like that if our input speed is decrease than 10ns then spike output value is near about 1v. So this 1v output can turn-on other MOS circuit. M9 and M10 are act as differentiator for Vin+. M9 acts as MOS capacitor. And M10 act as MOS Resistor. PMOS is used as resistor because of mobility of hole is less than electron. So PMOS gives high resistance value. Now consider 1v positive and 1v negative spike comes at the input of M11 and M12. During positive spike M11 turns on and during negative spike M12 turns on. So current is flowing through that during short amount time. Here M13 and M14 transistor are in fixed bias. So current flowing through these two is constant. Whenever high current flow then drain node voltage is increase because of loading effect. So it can turn on the transistor M15 and M16 which is heavy current sink. Therefor near about 1mA dynamic current is flowing in the circuit during transition so our slew rate increases. There are total three main parts of the dynamic circuit differentiator, Comparator and heavy Current sink.

As shown in fig. 3 transistor M9 and M10 are work as differentiator for Vin+ M11, M12, M13, M14 are work as comparator for input and both M15 and M16 work as heavy current sink. For Vin- M18, M17 work as differentiator and rest part are same. By considering the load capacitance 20fF we proposed our design and calculating the (W/L) of the figure 3.

This section should provide enough detail to allow full replication of the study by suitably skilled investigators. Protocols for new methods should be included, but well-established protocols may simply be referenced. We encourage authors to submit, as separate supporting information files, detailed protocols for newer or less well-established methods.

An important aspect of all scientific research is that it be repeatable. This gives validity to the conclusions. The materials and methods section of a manuscript allow other interested researchers to be able to conduct the experience to expand on what was learned and further develop the ideas. It is for this reason that this section of the paper be specific. It must include a step-by-step protocol along with detailed information about all reagents, devices, and subjects used for the study. How the data was constructed, collected, and interpreted should also be outlined in detail, including information on all statistical tests used.

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3. Results and Discussions

After designing of the proposed circuit, we have evaluated its performance in terms of slew rate, amplification and input common mode range performance and the results are presented in this section. For simulation purpose, we have used HSPICE software with appropriate transistor model file. At first, we have simulated the proposed circuit for slew rate measurement. Slew rate is nothing but how fast output can swing without distortion. For this we are apply pulse (i.e . VIN2 VIN+ 0 PWL (0 -0.8 5N -0.8 6N 0.8 10N 0.8 11N -0.8 50N -0.8 51N -.1 100N -.1 101N .1 150N .1 151N -.1 200N -.1) having very small rise and fall time and checking the output with and without the dynamic bias circuits.

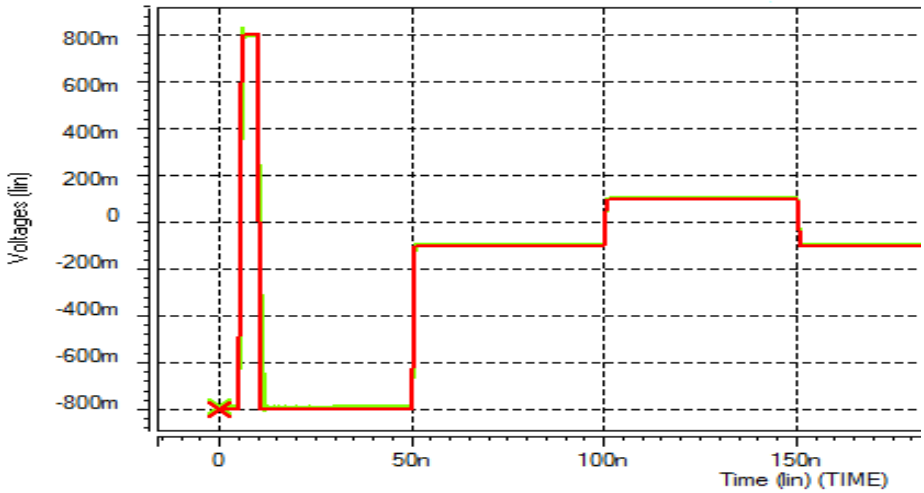

Figure 4: Simulation waveform for transient analysis for slew rate measurement

From simulation result, we find that the proposed Op-Amp slews at a rate of 1500 V/μs for rising signal and 900 V/μs for falling signal. This simulation result waveform is given in fig. 4 and fig.5. This slew rate is much higher than slew rate of ordinary Op-Amp. Thus this Op-Amp can be used in high very high frequency application such as audio and video communication transmission.

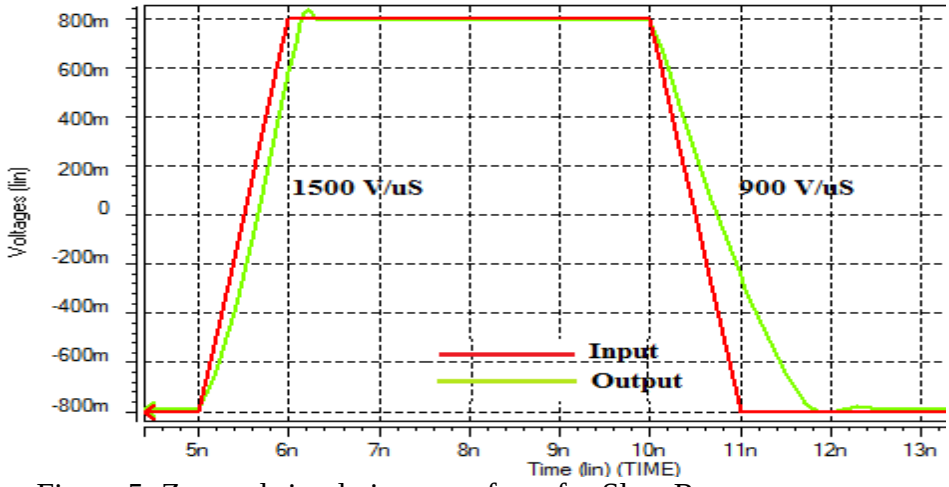

Figure 5: Zoomed simulation waveform for Slew Rate measurement

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Now we have to also consider other parameter of op-amp that is not to be degrading by after applying the dynamic bias circuit. For open loop gain calculation we apply a sinusoidal signal (VIN1 VIN- 0 SIN (0 100u 1K) AC 1.0) at the input of op-amp with 20fF load capacitor and 1.0 AC magnitude. For ICMR we apply DC input (. DC VIN1 -0.7 0.8 1000U) at the input terminal with stepping of 1mv

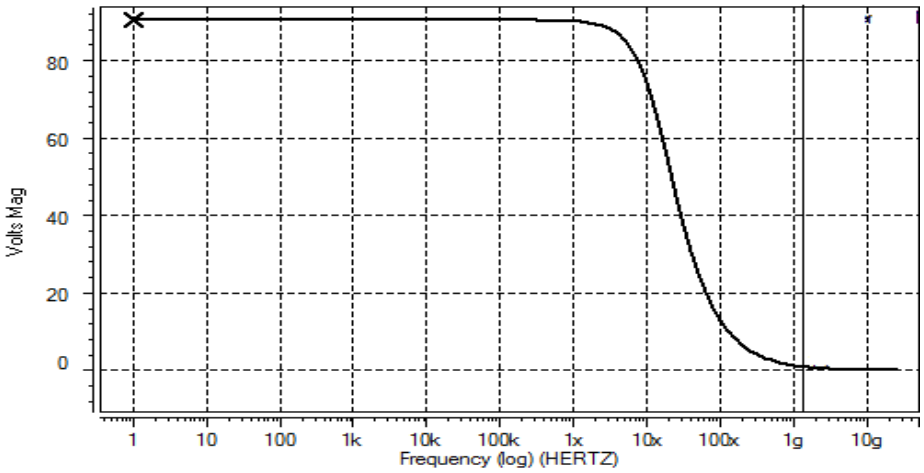

Figure 6: Gain Vs Frequency Plot of proposed Op-Amp

From Gain Vs frequency plot given in fig. 6, we can see that the gain of the proposed Op-Amp is 90.4 dB and the unity gain bandwidth (UGB) is found to be 1.27 GHz. This is again suitable for audio and video transmission applications.

After simulating for slew rate and gain calculation, we have simulated the proposed Op-Amp for input common mode voltage range (ICMR) calculation. A larger ICMR range is always required for a good dynamic amplification range. For ICMR calculation, here we keep the Op-Amp in a unity-gain non-inverting configuration and VDD/VSS is ±1.0 V. It can be seen that the op amp is ground sensing state. From ICMR simulation curve given in fig. 7, we found that the input common mode range (ICMR) of the proposed Op-Amp is -800 mV to +900 mV. This is a very good range for dual power supply of +1.0 V and -1.0 V.

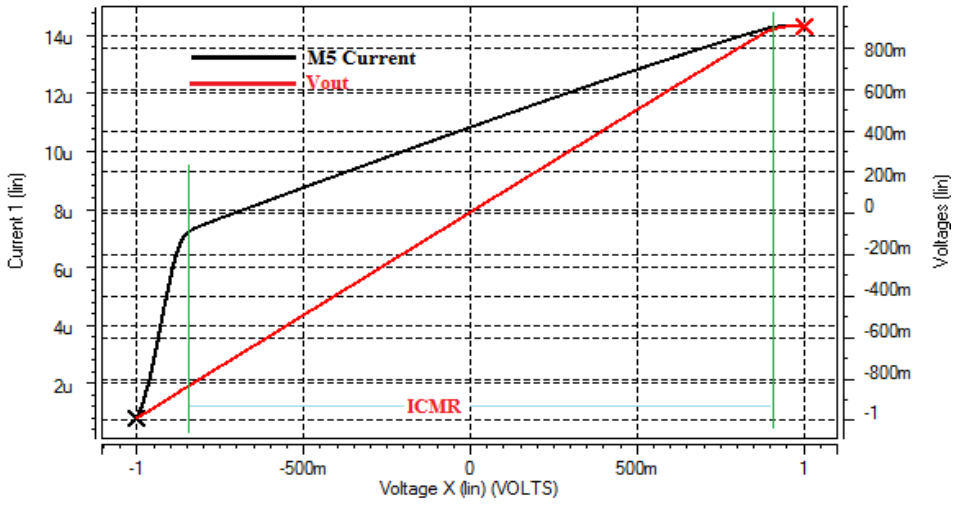

Figure 7: ICMR calculation of proposed Op-Amp

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4. Conclusions and Recommendations

After doing all the simulation and measurement, we come to know that, the proposed slew-rate boosting technique also obtains an increase of gain and bandwidth; a proper design optimization significantly reduces the extra power needed. The benefits of the proposed method can be quantified by two figures of merit, defined in [6], that measure the power effectiveness in achieving bandwidth and slew-rate. The proposed op amp has a power consumption of 661.83 µW. It has a dual supply voltage of -1.0V and 1.0V. The input common mode range (ICMR) of the proposed Op-Amp is -800 mV to +900 mV. The op amp has a slew rate of 1.5 KV/µs. Voltage gain of the op amp is 90.4dB with a unity gain bandwidth (UGB) of 1.27 GHz. This Op-Amp is suitable for audio and video transmission applications.

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